

S/N 09/874,894

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: William Jones et al.

Examiner: Thong Q. Le

Serial No.: 09/874,894

Group Art Unit: 2818

Filed: June 5, 2001

Docket: 303.764US1

Title:

METHOD OF CHARACTERIZING A DELAY LOCKED LOOP

9/11
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11-19-02

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on August 5, 2002. Please amend the above-identified patent application as follows.

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IN THE TITLE

Please delete the current title and replace with the following:

--CONTROLLER FOR DELAY LOCKED LOOP CIRCUITS--

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning at page 12, line 1 is amended as follows:

Between times T0 and T2, both of the [B_ACT-0] B_ACT-0* and EN_PSA-0 signals are LOW causing both inputs of NOR gate 410 to go LOW which forces a HIGH to the output of NOR gate 410 at line 406-0. This means the FREEZE-0 signal is HIGH forcing the output of NOR gate 420 at line 422 LOW. When one of the inputs, (e.g., on line 422) of NAND gate 424 is LOW, its output on line 430 is forced HIGH. Thus, between times T0 and T2, the STOP_PD signal is activated HIGH. The activated STOP_PD disables the shifting operation of the DLL, such as DLL 201 of Figure 2, during the ACTIVE mode.

The paragraph beginning at page 12, line 9 is amended as follows:

In Figure 4, the STOP_PD is HIGH when one of the FREEZE 0-3 signals is HIGH. However, one of the FREEZE 0-3 * is returned LOW a predetermined time after one of the corresponding EN_PSA 0-3 signals is activated HIGH. For example, in Figure 5, between times

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